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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,101	03/13/2007	Sacha Romier	DE03 0228 US1	8087

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EXAMINER	
HUYNH, PHUONG	

ART UNIT	PAPER NUMBER
2857	

NOTIFICATION DATE	DELIVERY MODE
04/02/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/562,101	ROMIER ET AL.	
	Examiner	Art Unit	
	PHUONG HUYNH	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/28/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Holloway et al. (hereinafter "Holloway") (US Patent No. 6,183,131).

Regarding claim 1, Holloway discloses an arrangement on a semiconductor chip for calibrating a temperature setting curve having

a signal generation unit for providing a first signal which is proportional to the actual temperature of the chip, whereby a signal offset creatable by the signal generation unit, which is combined with the first signal defining second signal [see Holloway: col. 11, lines 15-50];

a temperature extraction unit [A/D and summing circuits 114] receiving the first signal and the second signal calculating a first temperature point based on the first signal and a second temperature point based on the second signal, wherein

the second temperature point is a virtual [computed/calculated Tout(K), or Tout(C)]temperature [see Holloway: col. 7, lines 7-67, lines col. 11, line 40-col. 12, line 6].

Regarding claim 2, Holloway discloses that the first signal which is proportional to the actual temperature of the chip, is a current, voltage or a frequency [see Holloway: col. 11, lines 15-40].

Regarding claim 3, Holloway discloses that the first signal and the second signal are convertible into digital signals, whereby the extraction unit calculates the first and second temperature points for calibrating the temperatures setting curves [see Holloway: col. 11, line 40-col. 12, line 6].

Regarding claim 4, Holloway discloses a method for calibrating a temperature setting curve of a temperature sensor arrangement on a semiconductor chip, the method comprising:

reading a first signal which is proportional to an actual temperature of the semiconductor chip [see Holloway: col. 11, lines 15-40]; generating a signal offset, which is combined with the first signal defining a second signal [see

Holloway: col. 11, lines 40-47]; and extracting a first temperature from the first signal and a second virtual temperature from the second signal [see Holloway: col. 7, lines 7-67; col. 11, line 45-col. 12, line 25].

Regarding claim 5, Holloway discloses whereby the first actual temperature and the second virtual temperature are used for providing calibration parameters to the semiconductor chip [see Holloway: col. 7, lines 7-67; col. 11, line 45-col. 12, line 6].

Regarding claim 6, Holloway discloses whereby calculating calibration parameters can be performed on-chip *or* off-chip [see Holloway: Abstract; col. 7, lines 7-67; col. 11, line 45-col. 12, line 6].

Regarding claim 7, Holloway discloses whereby additional offsets are provided for calculating more than two temperature points and calibrating a non-linear temperature setting curve [see Holloway: col. 2, lines 6-20; col. 11, line 40-col. 12, line 25].

Regarding claim 8, Holloway discloses that whereby the signal offset is subtracted from the first signal or added to the first signal defining a second signal, which is provided to the temperature extraction unit [see Holloway: col. 11, line 45-col. 12, line 25].

Regarding claims 9 and 10, Holloway discloses that the second temperature point [computed Tout(K) or Tout(C)] does not exist in the semiconductor chip during calibration of the temperature setting curve [see Holloway: col. 11, lines 5-50].

Response to Arguments

2. Applicant's arguments filed 12/28/2008 have been fully considered but they are not persuasive.

Applicant argues that Holloway does not disclose "a **virtual** temperature" [which is calculated from a signal that is a combination of a signal representative of an actual temperature and a signal offset [see Applicant's Remarks: Pages 4-5].

Accordingly, Holloway, in col. 11, lines 5-15 discloses the **computed** [or virtual] output temperature Tout(K) orTout(C):

"The hyperbolic reference voltage Vhreff, which is the summed reference voltage Vref and correction voltage Vcorr, is provided to an amplifying circuit 110 that divides the hyperbolic reference voltage Vhreff with a scaling factor C. The scaling factor C provided by amplifying circuit 110 is used to generate the $C_{\beta cal}$ value derived in equation 14. Thus, amplifying circuit 110 generates a voltage

output signal Vo that is equivalent to the hyperbolic reference voltage Vhreff multiplied by the reciprocal of C. The voltage output signal V_o from amplifying circuit 110 is used to normalize the linearly-temperature-dependent voltage V_{TEMP} generated by thermometer circuit 104. Thus, both voltage output signal Vo and the linearly-temperature-dependent voltage V_{TEMP} are received by an A/D converter 112 that computes a digital fraction representing the ratio of the two voltages, i.e., V_{TEMP} /Vo, to a resolution of N bits. The A/D converter 112 produces a temperature output signal $T_{OUT\,(K)}$ in degrees Kelvin, which is therefore equivalent to: equation 19: $\mathbf{T_{OUT\,(K)} = T_{FS}\,(V_{TEMP}/Vo)}$ where T_{FS} the full scale digital output of the converter in Kelvin and may be chosen, e.g., to be 512 degrees Kelvin. A summing circuit 114 receives the temperature output signal $T_{OUT\,(K)}$ from A/D converter 112 and subtracts 273.15.degree. K, which is the Kelvin equivalent of 0^{o}C, to convert the temperature output signal $T_{OUT\,(K)}$ in degrees Kelvin to degrees Centigrade. Summing circuit 116 is used to add a temperature offset correction term K to the output signal from summing circuit 114 to produce the final temperature output signal $T_{OUT\,(C)}$ in degrees Centigrade. The temperature offset term K provided by summing circuit 116 is equivalent to the temperature correction offset term as derived in equation 17. The appropriate temperature offset correction term of the temperature sensor can easily be determined by adjusting the temperature sensor at ambient temperature to produce the appropriate output signal".

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHUONG HUYNH whose telephone number is (571)272-2718. The examiner can normally be reached on M-F: 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on 571-272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phuong Huynh
Examiner
Art Unit 2857

/P. H./
Examiner, Art Unit 2857
March 27, 2008

/Jeffrey R. West/
Primary Examiner, Art Unit 2857